What is claimed is:

1. A memory structure comprising;

a) a substrate;

b) a plurality of bottom electrodes overlying the substrate;

c) a plurality of top electrodes overlying the plurality of bottom electrodes;

d) a plurality of middle electrodes interposed between the plurality of bottom electrodes and the plurality of top electrodes, wherein each middle electrode forms a cross point with each bottom electrode and each top electrode as it crosses between the top electrode and the bottom electrode;

e) a first resistive memory material interposed between the plurality of bottom electrodes and the plurality of middle electrodes at each cross point;

f) a second resistive memory material interposed between the plurality of top electrodes and the plurality of middle electrodes at each cross point; and

g) a plurality of current sensing devices connected to the plurality of top electrodes, the plurality of bottom electrodes, or the plurality of middle electrodes.

2. The memory structure of claim 1, wherein the plurality of bottom electrodes comprise a bottom electrode material that allows for epitaxial formation of the perovskite material overlying the plurality of bottom electrodes.

3. The memory structure of claim 1, wherein the bottom electrode material is YBCO.

4. The memory structure of claim 1, wherein the bottom electrode material is platinum or iridium.

5. The memory structure of claim 1, wherein the first resistive memory material is a colossal magnetoresistance (CMR) material.

6. The memory structure of claim 1, wherein the first resistive memory material is $Pr_{1-x}Ca_xMnO_3$ (PCMO).

7. The memory structure of claim 1, wherein the first resistive memory material is $Gd_{1-x}Ca_xBaCo_2O_{5+5}$.

8. The memory structure of claim 1, wherein the plurality of current sensing devices is connected the plurality of middle electrodes, whereby the middle electrodes serve as shared bit lines.

9. The memory structure of claim 1, wherein the plurality of current sensing devices is connected to the plurality of top electrodes and the plurality of bottom electrodes and the plurality of middle electrodes serve as shared word lines.

10. A method of manufacturing a memory structure comprising the steps of:

a) providing a substrate;

b) depositing and planarizing a silicon oxide layer overlying the substrate;

c) depositing electrode material over the silicon oxide layer;

d) depositing resistive memory material, and a second electrode material overlying the electrode material;

e) patterning the second electrode material and the resistive memory material, stopping at the electrode material;

f) patterning the electrode material to form electrodes having a first orientation;

g) depositing silicon oxide and planarizing the silicon oxide stopping at the second electrode material;

h) depositing a electrode material; and

i) repeating steps (d) through (g), wherein step (f) patterning the electrode material forms electrodes at a second orientation, whereby a first two layer resistive memory array is formed.

11. The method of claim 10, further comprising repeating steps (b) through (i) to form a second two layer resistive memory array above the first two layer resistive memory array.

12. The method of claim 10, wherein the silicon oxide layer is between approximately 100nm and 200nm thick.

13. The method of claim 10, wherein the electrode material is YBCO.

14. The method of claim 10, wherein the electrode material is platinum or iridium.

15. The method of claim 10, wherein the resistive memory material is a perovskite material.

16. The method of claim 15, wherein the perovskite material is a colossal magnetoresistance (CMR) material.

17. The method of claim 16, wherein the perovskite material is $Pr_{1-x}Ca_xMnO_3$ (PCMO).

18. The method of claim 16, wherein the perovskite material is $Gd_{1-x}Ca_xBaCo_2O_{5+5}$.

19. The method of claim 10, wherein the step of planarizing the silicon oxide in step (g) comprises chemical mechanical polishing.

20. The method of claim 10, wherein first orientation and the second orientation produce electrodes arranged as a cross-point array.

21. The method of claim 10, further comprising forming peripheral circuitry prior to step (a).

22. The method of claim 11, further comprising forming vias to connect at least one electrode from the second two layer resistive memory array to at least one electrode from the first two layer resistive memory array.

23. The method of claim 22, wherein the connected electrodes form a common bit line.

24. The method of claim 22, wherein the connected electrodes form a common word line.